IN THE CLAIMS

Please amend the claims as follows:

1. (original) A method for designing an integrated circuit (IC) having IC parameters including process, circuit, and environmental design parameters comprising the steps of:

using design tools to layout and configure circuit macros making up said IC;

determining a leakage power for each of said circuit macros;

determining average leakage power sensitivities for said circuit macros to variations in said IC parameters;

selecting first parameters from said IC parameters in response to analyzing said average leakage power sensitivities; and

reducing a leakage power for one or more selected circuit macros of said circuit macros of said IC by modifying one or more of said first parameters.

2. (previously presented) The method of claim 1, wherein said circuit macros are classified as timing-non-critical circuit macros and timing-critical circuit macros, wherein said timing-non-critical circuit macros may have said IC parameters modified without significantly affecting an overall IC performance.

3. (previously presented) The method of claim 1, wherein said one or more selected circuit macros correspond to timing-non-critical circuit macros.

4. (previously presented) The method of claim 2 further comprising the step of determining a power dissipation margin as a difference between a first design power dissipation for said IC and a second power dissipation determined for said IC after said step of reducing said leakage power.

5. (original) The method of claim 4 further comprising the step of redesigning one of said circuit macros corresponding to said timing-critical circuit macros using said power dissipation margin to improve a performance of said redesigned circuit macro while keeping said overall IC power substantially equal to or below said first design power dissipation for said IC.

6. (previously presented) The method of claim 1, wherein said average leakage power sensitivity is determined by a method comprising the steps of:

determining occurrence probabilities for each input node of said circuit macros;

calculating state occurrence probabilities for each cell within said circuit macros;

retrieving predetermined leakage data and leakage power sensitivity data as a function of said IC parameters for cell inputs for said circuit macros from the cell library;

calculating an average leakage current for said circuit macros in response to said leakage data from said retrieving step, said occurrence probabilities for each of said input nodes of said circuit macro, and said state occurrence probabilities of each cell within said circuit macros;

calculating an average leakage power sensitivity for each circuit macro corresponding to each of said IC parameters in response to the leakage power sensitivity data from said retrieving step, said occurrence probabilities for each of said input nodes of said circuit macro, and said state occurrence probabilities of each cell within said circuit macros; and

saving average leakage power sensitivity data for each of said IC parameters for each circuit macro for use in optimizing said IC design.

7. (previously presented) The method of claim 6, wherein said leakage data and said leakage power sensitivity data for said IC parameters for said cell inputs are predetermined by using circuit analysis and circuit simulation tools.

8. (original) The method of claim 6, wherein said step of calculating said average leakage current uses a method comprising the steps of:

multiplying leakage currents for each logic state of each node of each cell of said circuit macro times corresponding logic state occurrence probabilities for each of said nodes generating a node leakage current for each node of each cell;

summing said node leakage current across each node of said cell generating cell leakage currents; and

summing said cell leakage currents across each cell generating said average macro leakage current.

9. (previously presented) The method of claim 6, wherein said step of calculating said average leakage power sensitivity for a parameter P of said IC parameters uses a method comprising the steps of:

multiplying a leakage power sensitivity for said parameter P for each logic state of each node of each cell of said circuit macro times corresponding logic state occurrence probabilities for each of said nodes generating a node leakage power sensitivity for each node of each cell;

summing said node leakage power sensitivities across each node of said cell generating a cell leakage power sensitivity for said parameter P; and

summing said cell leakage sensitivities across each cell of said macro generating said average macro leakage power sensitivity.

10. (previously presented) The method of claim 6 further comprising the step of outputting said saved leakage power sensitivity data during IC design in response to a designer request to evaluate affects of modifying said IC parameters to reduce a macro leakage current.

11. (original) A computer program product for determining an average macro leakage power sensitivity for an IC parameter, said computer program product embodied in a machine readable medium, including programming for a processor, said computer program comprising a program of instructions for performing the program steps of:

using design tools to layout and configure circuit macros making up said IC;

determining a leakage power for each of said circuit macros;

determining average leakage power sensitivities for said circuit macros to variations in said IC parameters;

selecting first parameters from said IC parameters in response to analyzing said average leakage power sensitivities; and

reducing a leakage power for one or more selected circuit macros of said circuit macros of said IC by modifying one or more of said first parameters.

12. (previously presented) The computer program product of claim 11, wherein said circuit macros are classified as timing-non-critical circuit macros and timing-critical circuit macros, wherein said timing-non-critical circuit macros may have said IC parameters modified without significantly affecting an overall IC performance.

13. (previously presented) The computer program product of claim 11, wherein said one or more selected circuit macros correspond to timing-non-critical circuit macros.

14. (previously presented) The computer program product of claim 12 further comprising the step of determining a power dissipation margin as a difference between a desired design power dissipation for said IC and a design power dissipation determined for said IC after said step of reducing said leakage power.

15. (original) The computer program product of claim 14 further comprising the step of redesigning one of said circuit macros corresponding to said timing-critical circuit macros using said power dissipation margin to improve a performance of said redesigned circuit macro while keeping said overall IC power substantially equal to or below said desired design power dissipation for said IC

16. (previously presented) The computer program product of claim 11, said average leakage power sensitivity is determined by a method comprising the steps of:

determining occurrence probabilities for each input node of said circuit macros;

calculating state occurrence probabilities for each cell within said circuit macros;

retrieving predetermined leakage data and leakage power sensitivity data as a function of said IC parameters for cell inputs for said circuit macros from the cell library;

calculating an average leakage current for said circuit macros in response to said leakage data from said retrieving step, said occurrence probabilities for each of said input nodes of said circuit macro, and said state occurrence probabilities of each cell within said circuit macros;

calculating an average leakage power sensitivity for each circuit macro corresponding to each of said IC parameters in response to the leakage power sensitivity data from said retrieving step, said occurrence probabilities for each of said input nodes of said circuit macro, and said state occurrence probabilities of each cell within said circuit macros; and

saving average leakage power sensitivity data for each of said IC parameters for each circuit macro for use in optimizing said IC design.

17. (previously presented) The computer program product of claim 16, wherein said leakage data and said leakage power sensitivity data for said IC parameters for said cell inputs are predetermined by using circuit analysis and circuit simulation tools.

18. (original) The computer program product of claim 16, wherein said step of calculating said average leakage current uses a method comprising the steps of:

multiplying leakage currents for each logic state of each node of each cell of said circuit macro times corresponding logic state occurrence probabilities for each of said nodes generating a node leakage current for each node of each cell;

summing said node leakage current across each node of said cell generating cell leakage currents; and

summing said cell leakage currents across each cell generating said average macro leakage current.

19. (previously presented) The computer program product of claim 16, wherein said step of calculating said average leakage power sensitivity for a parameter P of said IC parameters uses a method comprising the steps of:

multiplying a leakage power sensitivity for said parameter P for each logic state of each node of each cell of said circuit macro times corresponding logic state occurrence probabilities for each of said nodes generating a node leakage power sensitivity for each node of each cell;

summing said node leakage power sensitivities across each node of said cell generating a cell leakage power sensitivity for said parameter P; and

summing said cell leakage sensitivities across each cell of said macro generating said average macro leakage power sensitivity.

20. (currently amended) The computer program product of claim 16 further comprising the step of outputting said saved leakage power sensitivity data during IC design in response to a designer request to evaluate affects of modifying said IC parameters to reduce a macro leakage current.